Please amend the claims as follows:

1. (Currently amended) A method of operating a memory management system adapted to process linked list data files received by a packet router; said memory management system comprises a plurality of low storage capacity high speed memories and a lower speed high storage capacity bulk memory, said high speed memories have a first data rate, said bulk memory has a second data rate lower than said first data rate, said system further comprises an access flow regulator for generating requests received from said packet router for the reading and writing of linked list data files by said memories, said access flow regulator defines an interface between said packet router and said memory management system, said method comprises the steps of:

initiating the writing of a linked list in said high speed memories by transmitting a write request from said access flow regulator to said high speed memories;

writing a head buffer and a tail buffer and at least one intermediate buffer of said linked list into said high speed memories; and

transferring said at least one intermediate buffer from said high speed memories to said bulk memory while leaving the head buffer and the tail buffer in said high speed memories.

2. (Currently amended) A method of operating a memory management system adapted to process linked list data files received by a packet router; said memory management system comprises a plurality of low storage capacity high speed memories and a lower speed high storage capacity bulk memory, said high speed memories have a first data rate, said bulk memory has a second data rate lower than said first data rate, said system further comprises an access flow regulator for generating requests received from said packet router for the reading and writing of linked list data files by said memories, said access flow regulator defines an interface between said packet router and said memory management system, said method comprises the steps of:

transmitting a read request for a specified linked list from said access flow regulator to said high speed memories containing buffers of said specified linked list;

reading the head buffer of said specified linked list;

transferring said at least one intermediate buffer of said linked list from said bulk memory to one of said high speed memories;

designating the intermediate buffer transferred to in said one high speed memory as the replacement head buffer of said specified linked list;

reading out said intermediate buffer of said specified linked list from said one high speed memory; and

transmitting said read out buffers of said specified linked list to said access flow regulator.

3. (Currently amended) The method of claim 1 further including the step of operating said system to concurrently ~~processes~~ process linked lists for a plurality of requests from said access flow regulator.

4. (Original) The method of claim 1 further including the step of operating said system to process buffers of a linked list stored in different ones of said high speed memories.

5. (Original) The method of claim 1 further including the step of operating said system to write a tail buffer as the first buffer written to a new linked list; and the step of reading the head buffer of a linked list first.

6. (Currently amended) The method of claim [[1]] 2 wherein said system further comprises a plurality of state controllers each of which is individual to one of said high speed memories, said system further comprises a request bus connecting said access flow regulator with said state controllers; said step of transmitting a read request includes the steps of:

operating said access flow regulator to select an idle high speed memory that is to receive said read request;

transmitting said read request from said access flow regulator over said request bus to the state controller individual to said selected high speed memory; and

operating said state controller to extend said read request to said selected high speed memory.

7. (Original) The method of claim 6 wherein said step of operating said state controller includes the further steps of:

determining the present occupancy level of said selected high speed memory;

transmitting said request to said high speed memory if said present occupancy level is not exceeded; and

requesting a connection to said bulk memory if said present occupancy level of said selected high speed memory is exceeded.

8. (Currently amended) The method of claim 6 wherein said system further includes a multiplexer, and an access bus connecting said state controllers with said multiplexer, said system further includes a bus connecting said multiplexer with said bulk memory, said method includes the further step of operating said multiplexer to:

receive a request from said state controllers for a connection to said bulk memory;

determine which one of a plurality of requesting state controllers is to be granted access to said bulk memory;

connect one of said requesting state controllers to said bulk memory; and control the operation of said <u>one</u> bulk memory in the transfer of data from said one high speed memory to said bulk memory; and

apply buffers of said linked list from said state controller to said multiplexer via said access bus.

9. (Currently amended) The method of claim [[1]] 2 wherein said step of transferring said buffers from said bulk memory includes the steps of:

reading out intermediate buffers of a linked list from said bulk memory to said high speed memories in a burst mode having a data rate substantially equal to the data rate of said high speed memories;

storing said read out buffers in said high speed memories; and

subsequently reading out buffers of said linked list from said high speed memories for transfer to said access flow regulator.

10. (Original) The method of claim 1 including the further steps of:

writing buffers to an existing linked list by transferring the existing tail of said existing link list from said high speed memories to said bulk memory; and

writing a new buffer as a new tail buffer of said existing link list in said high speed memories.

11. (Original) The method of claim 1 including the further steps of:

embodying said system into a network node having incoming and outgoing links;

applying linked list buffers received by said links to said access flow regulator; and

processing said buffers by said memories to control the data throughput of said network node.

12. (Original) The method of claim 6 wherein said step of operating said state controller includes the further steps of:

concurrently receiving buffers of multiple linked lists;

separating the buffers of multiple linked lists directed to said access flow regulator; and

extending multiple accesses received by said access flow regulator to said high speed memories.

13. (Currently amended) The method of claim 6 wherein said step of operating said state controller includes the further steps of:

responding [[the]] <u>to</u> each received request to determine the present occupancy level of the high speed memory individual to said state controller;

extending said access to said associated high speed memory if said present occupancy level is not exceeded; and

signaling said access flow regulator to buffer said request if said present occupancy level is exceeded.

14. (Currently amended) The method of claim [[9]] 12 wherein said step of operating said state controller includes the further steps of:

controlling transfer of a buffer from said high speed memory in a burst mode to said bulk memory; and

controlling transfer of a buffer from said bulk memory to said high speed memory.

15. (Original) The method of claim 14 wherein said step of operating said state controller includes the further steps of:

determining whether said bulk memory is idle when a transfer is requested;

extending said buffers to said bulk memory if idle; and

buffering said transfer if said bulk memory is busy.

16. (Currently amended) The method of claim 8 wherein said step of operating said multiplexer includes the further steps of:

determining which one of a plurality of bidding high speed memories is to [[by]] be granted access to said bulk memory; and

buffering the requests of other ~~buffers in said one high speed memory~~ high speed memories.

17. (Currently amended) The method of claim 9 wherein said step of ~~operating said multiplexer~~ transferring said buffers includes the further steps of:

determining the identity to the high speed memory to which a buffer is to be directed from said bulk memory; and

controlling the transfer of said buffer in a burst mode from said bulk memory to said identified high speed memory.

18. (Currently amended) The method of claim 1 comprising the further steps of:

generating a signal unique to each high speed memory indicating the busy / idle state of each said high speed memory;

extending each generated busy/ idle signal to said access flow regulator;

operating said access flow regulator to receive requests for the writing or reading of linked lists by said high speed memories;

operating said access flow regulator in response to the receipt of a request to read said busy / idle signals generated by said high speed memories;

operating said access flow regulator to response to said reading to identify an idle one of said high speed memories; and

operating said access flow regulator for extending a request for the reading or writing of a data file to said idle one high speed memory.

19. (Currently amended) A memory management system adapted to process linked list data files received by a packet router; said memory management system comprises:

a plurality of high speed low storage capacity memories and a lower speed high storage capacity bulk memory, said high speed memories have a first data rate and said bulk memory has a second data rate lower than said first data rate;

an access flow regulator for generating requests received from said packet router for the reading and writing of linked list data files by said memories; said access flow regulator defines an interface between said packet router and said memory management system;

apparatus for initiating the writing of a linked list in said memories by transmitting a write read request from said access flow regulator to an idle one of said high speed memories;

apparatus for writing a head buffer and a tail buffer and at least one intermediate buffer of said linked list into said high speed memories;

apparatus for transferring said at least one intermediate buffer of said linked list from said high speed memories to said bulk memory while leaving the head buffer and the tail buffer of said linked list in said high speed memories;

apparatus for subsequently transmitting a request for the reading of said linked list from said access flow regulator to said high speed memories;

apparatus for reading the head buffer of said linked list in one of said high speed memories;

apparatus for transferring said at least one intermediate buffers of said linked list from said bulk memory to said high speed memories;

apparatus for designating the transferred buffer in said high speed memories as a new head buffer;

apparatus for subsequently reading out said head buffer and said tail buffer as well as said intermediate buffers from said high speed memories; and

apparatus for transmitting said read out buffers of said linked list to said access flow regulator.

20. Currently amended) The memory management system of claim 19 further comprising:

apparatus including said memories for generating a signal unique to each high speed memory indicating the present busy / idle state of each high speed memory;

apparatus for extending ~~said signals~~ each generated busy / idle signal to said access flow regulator;

apparatus including said access flow regulator for receiving a request for the writing or reading of linked lists by said high speed memories;

apparatus including said access flow regulator for reading said busy / idle signals in response to the receipt of said request;

apparatus including said access flow regulator for determining the current busy / idle state of each of said high speed memories in response to said reading;

apparatus including said access flow regulator for granting a request for the reading or writing of a linked list by said high speed memory in response to a determination that one of said memories is currently idle.